

2900 Semiconductor Drive, Santa Clara, California 95051



DECEMBER

1969



MM421/MM5211024 bit read only memory

general description

The MM421/521 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication.

features

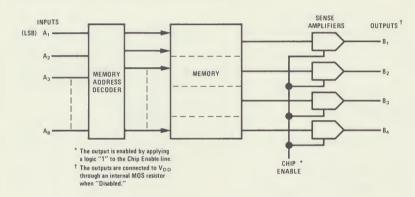
- Bipolar Compatibility
- High Speed Operation <1.0 µs TYP

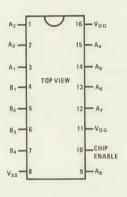
- Static Operation no clocks required
- Common Data Bussing output wire AND capability
- Chip Enable Output Control

applications

- Code Conversion
- Random Logic Synthesis
- Table Look-up
- Character Generators
- Micro-programming

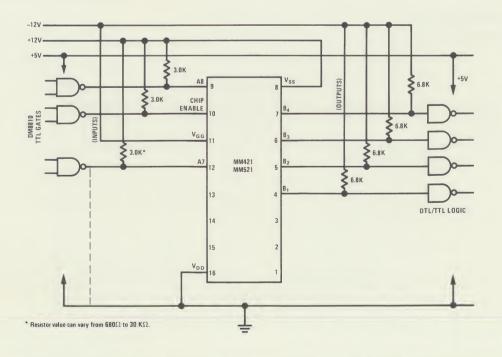
block and connection diagrams





typical application

256 x 4 Bit ROM Showing TTL Interface



absolute maximum ratings

electrical characteristics (Note 1)

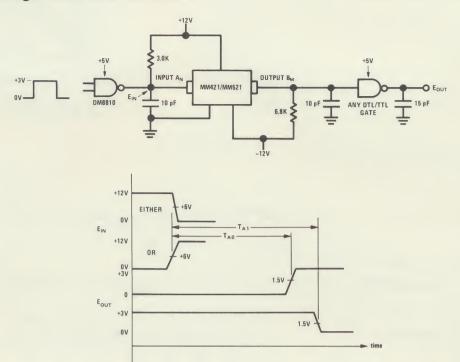
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels MOS to MOS Logical "1" Logical "0"	1 M Ω to GND Load	V _{SS} - 1.0		V _{SS} - 9.0	V
MOS to TTL Logical "1" Logical "0"	$6.8~k\Omega$ to V_{GG} Plus One Standard Series 54/74 Gate Input	+2.5		+0.4	V
Input Voltage Levels Logical ''1'' Logical ''0''		V _{SS} - 2.0		V _{SS} -8.0	V
Power Supply Current Requirements V _{SS} V _{GG} (Note 2)	T _A = 25°C		20	35 1	mΑ μΑ
Input Leakage	V _{IN} = V _{SS} -12V			1	μΑ
Input Capacitance	f = 1.0 MHz V _{1N} = 0V		5		pF
Address Time (Note 3) T _{A1} T _{A0}	T _A = 25°C See Timing Diagram		550 600	1000 1000	ns ns
Output AND Connection .	MOS Load TTL Load			4 10	

Note 1: These specifications apply for VSS = +12V \pm 10% and VGG = -12V \pm 10% and TA = -55°C to +125°C (MM421), TA = -25°C to 70°C (MM521) unless otherwise specified.

Note 2: The $V_{\hbox{GG}}$ supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

timing diagram/address time

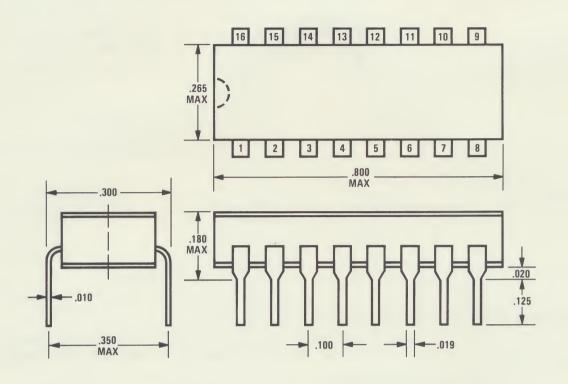


pattern selection form

The memory contents for individual requirements must be submitted on an $8-1/2^{\prime\prime}$ X 11 $^{\prime\prime}$ size of the form below. For copies of MM421/521 Bit Selection form, write or call local National Sales office or National, Santa Clara.

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6		44	82	120			158		196		230	
7		45	83	12			159		197		231	
8		46	84	12			160		198		232	
9		47	85	12	3		161		199		233	
10		48	86	12	1		162		200		234	
11		49	87	12	5	П	163		201		235	
12		50	88	12	5		164		202		236	
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18		56	94	13	2		170		208		242	
19		57	95	13	3		171		209		243	+++
20		58	96	13	1		172		210	+	244	H
21		59	97	13	5	\perp	173		211		245	+++
22	+++	60	98	13	5	\perp	174		212		246	+++
23		61	99	13	+	Ш	175	1	213		247	+++
24	+	62	100	13		Ш	176		214	+++	248	+++
25		63	101	13	-	+-	177		215	+++	249	+++
26	+	64	102	14	-	\perp	178		216	+++	250	+++
27		65	103	14		H	179		217	+	251	+++
28	+++	66	104	14		H	180		218	+++	252	+++
29		67	105	14	-		181		219		253 254	+++
30		68	106	14		1	182		220	+++	255	+++
31	+	69	107	14		+	183	-	221		255	
32		70	108	14	+++	+	184	+	222	+++		
33	+	71	109	14		-	185	-	223	+++		
34	++++	72	110	14		-	186	++	224		J	
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36	+	74	112	15		+	188	-	FOR	NATIONAL	SEMICONI	DUCTOR
37	+++	75	113	15		+	189	-			ONLY	
38		76	114	15	2		190		DEVI	CE NO M	M - 21-	

physical dimensions



Hermetic Dual-In-Line Package
Order Number MM421 or MM521

National Semiconductor Corporation

2900 Semiconductor Drive, Santa Clara, California 95051 (408) 732-5000 / TWX (910) 339-9240



1M420/MM520

256



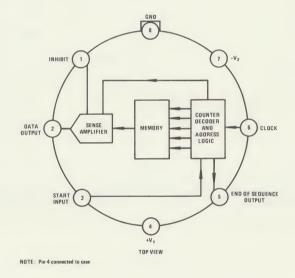
MM420/MM520 256 bit read only memory

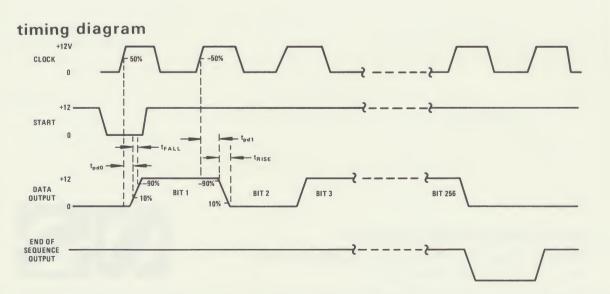
general description

The MM420 and MM520 are 256-bit read only memories which have a clocked serial output. They are ideally suited for character generators, read only drum type memories, micro programming for control and operating programs, and memory systems that are completely interrogated upon command. The device is constructed on a single silicon chip using MOS P-channel enhancement mode transistors. It contains all counters and

decoders for addressing the memory array. A sense amplifier on the chip provides improved speed and noise immunity. An end of sequence output is provided to allow expanding the serial bit length without external components. The memory contents are programmed to individual customer specification during the metalization process of device fabrication.

schematic and connection diagram





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MM420/MM520 256 bit memory

absolute maximum ratings

electrical characteristics (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Logical ''1'' Output Voltage				+1	V
Logical ''0'' Output Voltage		+10			V
Logical "1" Input Voltage				+3.0	V
Logical ''0'' Input Voltage		+9.3			V
Power Dissipation			100		mW
Maximum Clock Frequency			0.5		MHz
Minimum Clock Frequency		DC			
Transient Performance					
t _{RISE}	See Timing Diagram		0.5		μs
t _{FALL}	$C_{LOAD} = 10 pF$		0.2		μs
t _{pd1}			1.5		μs
t _{pd0}			1.5		μs

NOTE 1: These specifications apply for $+V_1 = 12V \pm 10\%$ and $-V_2 = -12V \pm 10\%$, unless otherwise specified.

National Semiconductor Corporation

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DECEMBER 1969



MM422/MM522 1024-bit read only memory

general description

The MM422/MM522 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a nonvolatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

features

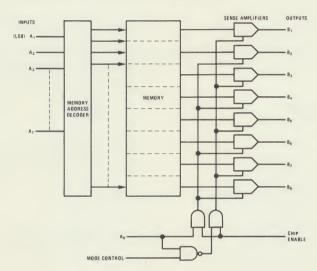
- Bipolar Compatibility
- High Speed Operation $< 1.0 \,\mu s$ TYP.

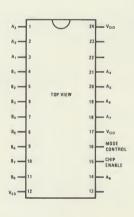
- Static Operation no clocks required
- Common Data Bussing output wire AND capability
- Chip Enable Output Control

applications

- Code Conversion
- Random Logic Synthesis
- Table Look-up
- Character Generators
- Micro-programming

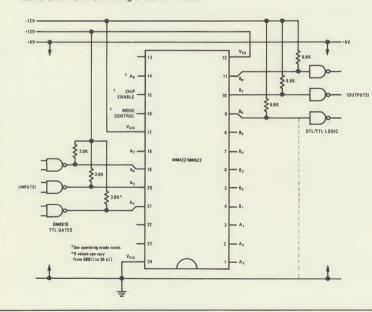
block and connection diagrams





typical application

128-8 Bit ROM Showing TTL Interface



Operating Modes

128x8 ROM connection Mode Control - Logic "0"

256x4 ROM connection

Mode Control - Logic "1" - Logic "0" Enables the odd

(B₁...B₇) outputs

- Logic "1" Enables the even

 $(B_2 ... B_8)$ outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled.

absolute maximum ratings

electrical characteristics (Note 1)

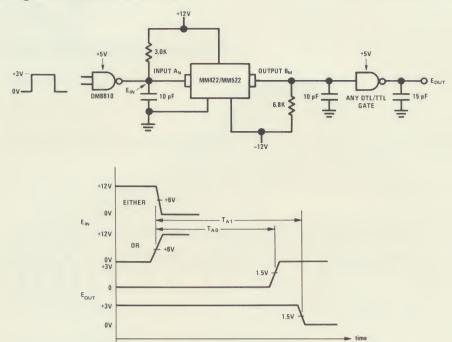
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels MOS to MOS Logical "1" Logical "0"	1 M Ω to GND Load (Note 2)	V _{SS} -1.0		V _{SS} -9.0	V
MOS to TTL Logical "1" Logical "0"	6.8 k Ω to V $_{\rm GG}$ Plus One Standard Series 54/74 Gate Input	+2.5		+0.4	V V
Input Voltage Levels Logical ''1'' Logical ''0''		V _{SS} -2.0		V _{SS} -8.0	V
Power Supply Current Requirements V _{SS} V _{GG} (Note 2)	$T_A = 25^{\circ}C$		20	35 1	mΑ μΑ
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μΑ
Input Capacitance	f = 1.0 MHz V _{IN} = 0V		5		pF
Address Time (Note 3) T _{A1} T _{A0}	T _A = 25°C See Timing Diagram		550 600	1000 1000	ns ns
Output AND Connection	MOS Load TTL Load			4 10	

Note 1: These specifications apply for V_{SS} = +12V \pm 10% and V_{GG} = -12V \pm 10% and T_A = -55°C to +125°C (MM422), T_A = -25°C to 70°C (MM522) unless otherwise specified.

Note 2: The $V_{\mbox{GG}}$ supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

timing diagram/address time

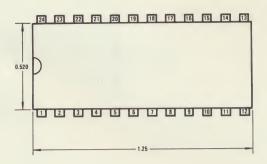


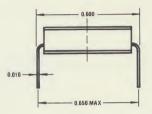
pattern selection form

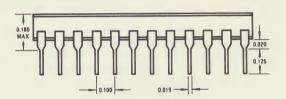
The memory contents for individual requirements must be submitted on an $8-1/2^{\prime\prime} \times 11^{\prime\prime}$ size of the form below. For copies of the MM422/522 Bit Selection form, write or call local National Sales office or National, Santa Clara.

7.1T			Phon	e (408	3) 245	-2310			TWX 910-	339-9240								PA	TTE	RN SELI		ON					
NAME																				D	TE						
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	TH	E F	OL	LOW	INC	P.	TT	ERN	IS RE	QUIRED	(0)	4 MY	Y MN	4422	-5	5 ° C	TC) +	125°	C □ ; N	M522	2-2	5°	СТО	+70	o° c	□;
ADD -			оит	PUT	COL)E			H INPL	ADD-	ESS	: IN	PUT	AD	DRE	SS IS	A7	, A6	, A5,	A4. A3. A	12, A	1.	OUT	PUT	CODE	_	
RESS	B8	В7	В6	В5	В4	B3	B2	В1		ADD- RESS	88	В7	B6	B5	В4	В3	В2	В1		ADD- RESS	В8	В7	В6	B5	B4 B	3 B2	B1
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33										76										119							
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35										78										121							1
36										79						4				122					4	+	-
37										80						4	1			123					4	-	-
38_										81					-	+	1			124					+	-	-
39		-			-					82						-	-	_		125					+	+	-
40	-		-							83				-	-	-+	-			126					+	+-	+
41					-					84 85					-	-	-	_		127							OR

physical dimensions







Hermetic Dual-In-Line Package
Order Number MM422 or MM522

National Semiconductor Corporation

2900 Semiconductor Drive, Santa Clara, California 95051 (408) 732-5000 / TWX (910) 339-9240



DECEMBER 1969



MM423/MM523 2048-bit read only memory

general description

The MM423/MM523 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

features

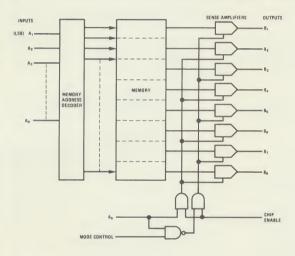
- Bipolar Compatibility
- High Speed Operation $-<1.0 \mu s$ TYP.

- Static Operation no clocks required
- Common Data Bussing output wire AND capability
- Chip Enable Output Control

applications

- Code Conversion
- Random Logic Synthesis
- Table Look-up
- Character Generators
- Micro-programming

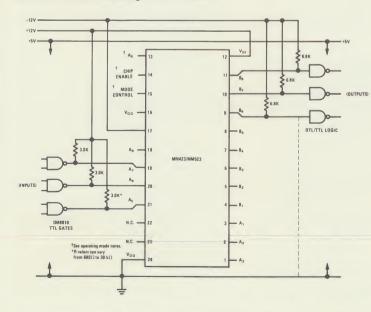
block and connection diagrams





typical application

256 x 8 Bit ROM Showing TTL Interface



Operating Modes

256x8 ROM connection Mode Control — Logic "0" A₉ — Logic "1"

512x4 ROM connection

Mode Control — Logic "1"

A₉ — Logic "0" Enables the odd

(B₁, B₃..., B₉) outputs

(B₁, B₃...B₉) outputs

- Logic "1" Enables the even
(B₂, B₄...B₈) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to $V_{D\,D}$ through an internal MOS resistor when "Disabled."

absolute maximum ratings

electrical characteristics (Note 1)

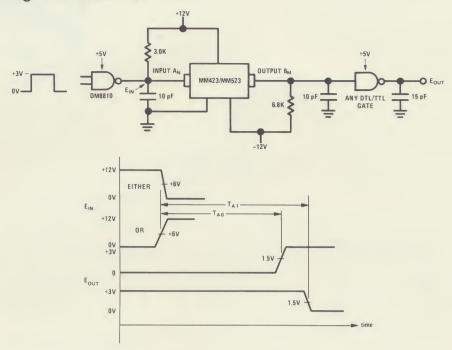
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels MOS to MOS Logical "1" Logical "0"	1 M Ω to GND Load	V _{SS} -1.0		V _{SS} -9.0	V
MOS to TTL Logical "1" Logical "0"	6.8 k Ω to V $_{\rm GG}$ Plus One Standard Series 54/74 Gate Input	+2.5		+0.4	V
Input Voltage Levels Logical "1" Logical "0"		V _{SS} -2.0		V _{SS} -8.0	V
Power Supply Current V _{SS} V _{GG} (Note 2)	T _A = 25°C		24	35 1	mΑ μΑ
Input Leakage	V _{IN} = V _{SS} -12V			1	μΑ
Input Capacitance	f = 1.0 MHz V _{IN} = 0V		5		pF
Address Time (Note 3) T _{A1} T _{A0}	See Timing Diagram		850 500	1500 1500	ns ns
Output AND Connection	MOS Load TTL Load			4 10	

Note 1: These specifications apply for VSS = +12V \pm 10% and VGG = -12V \pm 10% and TA = -55°C to +125°C (MM423), TA = -25°C to 70°C (MM523) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

timing diagram/address time

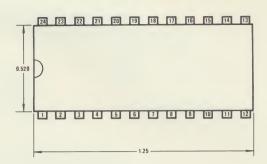


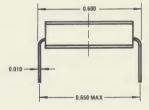
pattern selection form

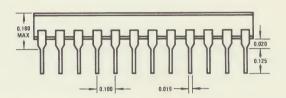
The memory contents for individual requirements must be submitted on an $8-1/2^{\prime\prime} \times 11^{\prime\prime}$ size of the form below. For copies of the MM423/523 Bit Selection form, write or call local National Sales office or National, Santa Clara.

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ADDRESS THRU A 188		UTPUT	CODE (3)		(21ADDRESS			DUTPU	T COD	E (3)		(2)ADDRESS		DUTP	UT	CODE	3)	
0	Τ̈́Τ	00 05	D4 B3		"	43	88	87	B6 B5	184	B3 B2	BI	86	88 8	7 86 1	35 8	34 B3	B2 I	81
1						44				\Box			87			\top			_
2						45							88						
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72				-								VE OUTPUT TING	FOR NA	TIONA	AL SEA	IICO	NDUC	TOR	7

physical dimensions







Hermetic Dual-In-Line Package
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MOS BRIEF 8

DIGITAL DISPLAY SYSTEMS

TTL-compatible MOS storage circuits solve a dilemma that has plagued display designers: the question of how to generate the display. Eliminating digital-to-analog conversion allows a data system to remain digital right up to the display drivers, but may exchange one economic headache for another. If the data source generates the digital control signal, its cost and that of communications links rise. Doing the job in the terminal, on the other hand, has made displays costly in the past.

MOS read-only memories reduce, to a few relatively inexpensive integrated circuits, the hardware required to convert a character communications code to signals that will control a display. Display rates fast enough for most applications can be achieved, when the MOS ROMs are controlled by bipolar logic circuits. And when the ROMs and bipolar ICs can be coupled directly, without the use of special voltage translators, the character generator becomes that much more inexpensive.

produce a display-control system, such as the one in Figure 3. This system adds data buffering, message storage and display refresh to the basic character-generation function.

Ordinarily, read-only memories are custom-made and programmed for special applications. A large order must be placed to amortize the setup costs and bring the price below 2d per bit. These ROMs are different. They are mass-produced as preprogrammed, off-the-shelf kits. Each kit contains

Two cases in point are shown in Figures 1 and 2.

The MOS read-only memories can be bought for

less than 2¢ per bit of storage. A small additional

investment in MOS registers and TTL counters will

are different. They are mass-produced as preprogrammed, off-the-shelf kits. Each kit contains three 1024-bit ROMs programmed to generate 64 alphanumeric display symbols when addressed by the ASCII code. The kit for raster-scan displays is SK0001 and the kit for vertical scanning is SK0002. Figure 4 shows how the characters in the

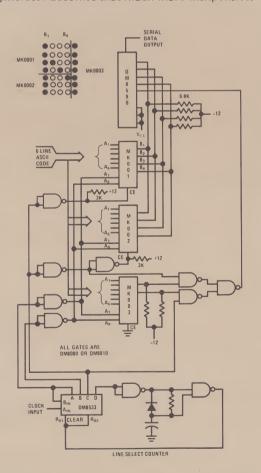


FIGURE 1. Raster-Scan MOS/TTL Display Character

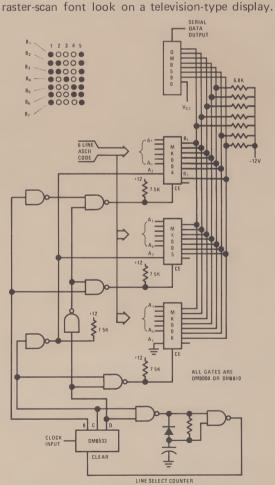


FIGURE 2. Character Generator for Tape Printers and Other Vertical-Scan Applications.

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NATIONAL SEMICONDUCTOR MOS GUIDE



PKG	TO-100 001-07	TO-100 TO-100 TO-100	SWITCH	DPDT SP4T 4PST DPDT	SP4T 3PST DPDT SP4T 4PST	DPDT SP4T 3PST MAX DISS (mW)	800 1500 1500	800 1500 1500 1500	52 purup resss
V _{GG} (V)	None None	None None None	PKG. TYPE	TO:100 TO:100 FLAT***	FLAT*** TO-100 TO-100 TO-100 FLAT***	FLATTTTFLATON	7 7 7 7	- 2 - 2	y include a 20 h
V _{DD} (V)	G N D D C C C C C C C C C C C C C C C C C			7 7 7 7	10 221	FE FE TC OFF STATE DISSIPATION (mW)	20 00	20 00	except that tire;
V _{SS} (V)	+ 10 + 10 + 10	+10 +10 +10	INPUT (DRAIN) CAPACITANCE	10 pF 10 pF 10 pF	6 pF 10 pF 10 pF 10 pF	10 pF 6 pF 10 pF			D6 respectivery.
POWER DISSIPATION mW/MHz/bit			ANCE -10V)	20 20 20 20 20 20 20 20 20 20 20 20 20 2	22 22 23 24 25 25 26 26 26 27 26 26 26 26 26 26 26 26 26 26 26 26 26	aaa	Y es Y es Y es	Yes Yes No	M406, and mms
PC DISSI mW///	0 1 0 1 5 1 5 1 5 1 5 1 5 1 5 1 5 1 5 1		ON RESISTANCE (VIN = -10V)	6000 6000 6000 6000 6000	\$000 \$000 \$000 \$000 \$000 \$000	6000 6000 6000 MAX REP RATE (MHz)	2 10 5	10	5V at reduced o
MAX OPER FREG (MHz)	200 ns 400 ns 400 ns	200 ns 400 ns 400 ns 2.0 MHz	INPUT (DRAIN) LEAKAGE	200 pA 200 pA 200 pA 200 pA	200 pA 200 pA 20 nA 20 nA 20 nA	20 nA 20 nA 20 nA 20 nA CURRENT (mA)	±300 ±500 ±1000 ±500	±300 ±500 ±1000 ±500	5°C to +125°C). = -5V, VSS = +1 but drive charact
NO. OF BITS	Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z	Z Z Z Z Z	ANALOG INPUT VOLTAGE			th ±10V ±10V ±10V \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$	12 – 30 12 – 30 12 – 30 12 – 30	12 – 30 12 – 30 12 – 30 12 – 30	ntical to Minary (–5) eration on VDD atibility and out
PRODUCT DESCRIPTION	ū	Dual 3 Input NOR Gate Dual 3 Exclusive OR Gate Dual Digital Multiplex Switch JK Flip Flop	PROD TYPE PRODUCT DESCRIPTION NO.	Dual Diff. Analog Switch Four Channel Analog Switch Four MOS Transistor Package DTL/TTL Compatible Dual Diff. Switch	Four Channel Analog Commutator Three MOS Transistor Package Dual Diff. Analog Switch Four Channel Analog Switch Four Channel Analog Switch Four MOS Transistor Package	DTL/TL Compatible Dual Diff. Switz Four Channel Analog Commutator Three MOS Transistor Package PRODUCT DESCRIPTION	ORIVERS Single Phase Clock Driver Two Phase Clock Driver Single Phase Clock Driver Two Phase Clock Driver Two Phase Clock Driver	C Single Phase Clock Driver C Two Phase Clock Driver C Single Phase Clock Driver C Two Phase Clock Driver	Middol, Middol, Middol, Middol, Middol, and Middol, ber delartice to Middol, Middol, and Anderson And
** PROD TYPE NO. #	LOGIC MM480 MM481 MM482	MM581 MM581 MM583		MM450 MM451 MM452 MH453	MM455 MM550 MM551 MM551	MM554 MM555 MM555 TYPE NO.	CLOCK NH0007 NH0012 NH0013	NH0007C NH0009C NH0012C NH0013C	on, mmbor, n erature Range Package is 14 IM400/500 Se Ind generation evices can be k
TEMP.* *	MIL	COM	TEMP.**	MIL	W00	TEMP	MIL	COM	*** Flat See N #Secor
PKG	0.99 0.07 0.099	TO:99 TO:99 TO:100	10.99 10.99 10.99 10.99 10.99	TO-100 DIP	TO-99 TO-99 DIP TO-100 TO-100	TO:99 TO:99 DIP DIP TO:100	TO-99 DIP DIP	TO-99 DIP DIP	010
\$ \$	+10 to -6 +10 to -6 +10 to -6	+10 to -6 +10 to -6 +10 to -6 +10 to -6 +5 to -12	+10 to -6 +10 to -6 +10 to -6 +10 to -6 +10 to -6	+10 to -6 +5 to -12	+10 to -6 +10 to -6 +10 to -6 +10 to -6 +5 to -12 +5 to -12	+10 to -6 +10 to -6 +10 to -6 +10 to -6 +5 to -12 +5 to -12			
V _{GG}	None None	None None -6	None None None	-12	-6 -6 -12 -12	-6 -6 -12 -12	-12 -12 -12	-12 -12 -12	-12
V _{DD} (V)	GND	GND GND GND None	GND GND GND GND	None	GND GND None None	GND GND None None	GND GND GND GND	GND GND GND GND	GND
V _{SS}	+10+ +10† +10†	+10++10++110++110++15	+10++10++10++10++10++10+	+10	+ 10 + 10 + 10 + 5 + 5	+10 +10 +10 +10 +5 +5	+12 +12 +12	+12 +12 +12 +12	+12
POWER DISSIPATION mW/MHz/bit	0.88	0.0000	8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	0.3	6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6. 6	0. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.	100 mW Total 250 mW Total 250 mW Total 350 mW Total	100 mW Total 250 mW Total 250 mW Total 350 mW Total	250 mW Total/ Pkg 250 mW Total/ Pkg
MAX OPER FREQ (MHz)	0.1	0.1 0.1 0.1 0.1 0.1	0.1.0.1.0.0.1.0.0.1	1.0	0.1.0.1.0.1	0.1.0.0.1.0.1.0.0.1	0.25 1.0 1.0	0.25 1.0 1.0	0.1
NO. OF NO. OF BITS CLOCKS	5 5 5	2 2 2 2 2	000000	2 2					
NO. OF	50 50 100	200 200 128 192	50 100 100 200 200	128	32 49 88 89 49	32 64 8 8 64 64	256 1024 1024 2048	256 1024 1024 2048	2240
PRODUCT DESCRIPTION	DYNAMIC SHIFT REGISTERS MM400 Dual 25 bit Shift Register MM401 Dual 25 bit Shift Register MM402 Dual 50 bit Shift Register	Usa bo to Shift Register Dual 100 bit Shift Register Dual 100 bit Shift Register Dual 64 bit Accumulator/Register Triple 6044 bit Accumulator/Register	Dual 25 bit Shift Register Dual 25 bit Shift Register Dual 50 bit Shift Register Dual 50 bit Shift Register Dual 100 bit Shift Register Dual 100 bit Shift Register	MM510 Dual 64 bit Accumulator/Register MM5015‡ Triple 60+4 bit Accumulator/Register STATIC SHIFT REGISTERS	Dual 16 bit Shift Register Dual 32 bit Shift Register 8 bit Serial In-Parallel Out Register 8 bit Parallel In-Serial Out Register Dual 32 bit Shift Register Dual 32 bit Shift Register Split Clook	Dual 16 bit Shift Register Dual 32 bit Shift Register 8 bit Serial In-Parallel Our Register 8 bit Parallel Serial Our Register Dual 32 bit Shift Register Dual 32 bit Shift Register Split Clock	MM420 256 bit Function Generator MM421 1024 bit ROM (256.4) MM422 1024 bit ROM (128.8) MM423 2048 bit ROM (256.8 or 512.84)	256 bit Function Generator 1024 bit ROM (256 x 4) 1024 bit ROM (128 x 8) 2048 bit ROM (256 x 8 or 512 x 4)	3 Package Character Generator Kit ASCII 64 x 7 x 5 Raster Scan 3 Package Character Generator Kit ASCII 64 x 5 x 7 Vertical Scan
PROD TYPE NO.#	DYNAMIC MM400 MM401*	MM405 MM407 MM410 MM410	MM500 MM501* MM502 MM503 MM506	MM5015 [‡] STATIC SH	MM404 MM405 MM408 MM409 MM4050‡ MM4051‡	MM5054 MM505 MM509 MM5051#	READ ONL MM420 MM422 MM422	MM520 MM521 MM522 MM523	SK0001
TEMP.**		MIL	COM		MIL	COM	MIL	COM	



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